

深圳市阿美林电子科技有限公司 Shenzhen Amelin Electronic Technology Co. Ltd.	Doc.No.: AML550L3901	
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SPEC TITLE DOCUMENT CONTROL SPECIFICATION	EFFECTIVE DATE: 2017-02-23	

Specifications

TFT-LCD module

Model No: **AML550L3901**

For Customer's Acceptance	
Approved by	Comment

	Signature	Date
Prepared by		
Checked by		
Approved by		

Revision Record

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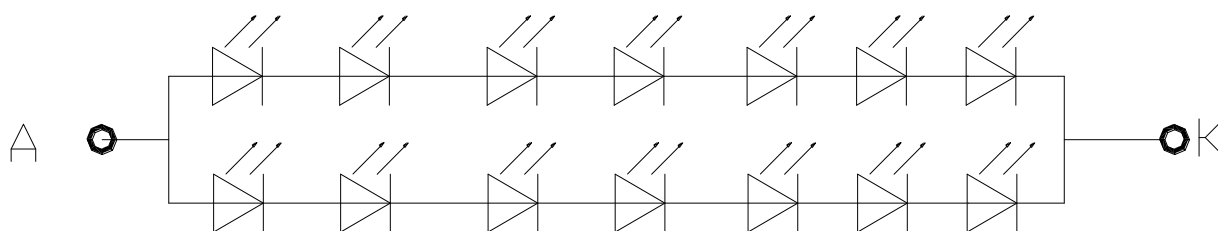
1. General linformation

ITEM	STANDARD VALUES	UNITS
LCD type	5.5" TFT	--
Dot arrangement	1080 (RGB) × 1920	dots
Driver IC	NT35532	--
Module size	70.84(W) x 129.01(H) x 1.49(T)	mm
Active area	68.04(W) x 120.96(H)	mm
Dot pitch	0.063(H) x 0.063(V)	mm
Operating temperature	- 20 ~ + 70	°C
Storage temperature	- 30 ~ + 80	°C
Back Light	14 White LED In Parallel	--
Weight	TBD	g

2 .Absolute Maximum Ratings

ITEM	Symbol	MIN	MAX	UNITS
Power supply voltage 1	VCC	2.8	3.3	V
Power supply voltage 1	IOVCC	1.8	3.3	V
Operating temperature	Topr	-20	+70	°C
Storage temperature	Tstg	-30	+80	°C
Humidity	RH	---	90%(Max40°C)	RH

3.Backlight Charasterics



Circuit Diagram
 $I_F = 2 \times 20\text{mA}$, $V_F = 21 - 22.4\text{V}$

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Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	Vf	21	22.4	23.8	V	If=40 mA	-
Supply Current	If	-	40	-	mA	-	-
Reverse Voltage	Vr	-	-	5	V	10uA	
Power dissipation	Pd	-	896	-	mW	-	
Luminous Intensity f or LCM		-	350	-	mCd/m²	If=40 mA	
Uniformity for LCM	-	80	-	-	%	If=40 mA	
Life Time	-	50000	-	-	Hr	If=40 mA	-
Backlight Color	White						

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5. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	GND	System Ground
2	IOVCC	Power Supply For LCD
3	NC	Not Control
4	RESET	Reset Signal
5	TE	Tearing Effect Output Signal
6	NC	Not Control
7	GND	Ground
8	D3P	Positive polarity of low voltage differential data 3
9	NC	Not Control
10	D3N	Negative polarity of low voltage differential data
11	GND	Ground
12	D2P	Positive polarity of low voltage differential data 2 signal
13	NC	Not Control
14	D2N	Negative polarity of low voltage differential data 2 signal
15	GND	Ground
16	CLKP	Positive polarity of low voltage differential clock signal
17	NC	Not Control
18	CLKN	Negative polarity of low voltage differential clock signal
19	GND	Ground
20	D1P	Positive polarity of low voltage differential data 1
21	NC	Not Control
22	D1N	Negative polarity of low voltage differential data
23	GND	Ground
24	D0P	Positive polarity of low voltage differential data 0
25	NC	Not Control
26	D0N	Negative polarity of low voltage differential data
27	GND	Ground
28	NC	Not Control
29	VCC	POWER SUPPLY FOR LCD(2.8V)
30	IOVCC	Power Supply For LCD
31	GND	Ground
32	LEDA	Power Supply For LED Backlight Anode Input
33	LEDA	Power Supply For LED Backlight Anode Input
34	LEDK	Power Supply For LED Backlight Cathode Input
35	LEDK	Power Supply For LED Backlight Cathode Input
36	GND	Ground
37	LEDPWM	PWM (Pulse Width Modulation) Signal Of LED
38	NC	Not Control
39	ID	LCM_ID

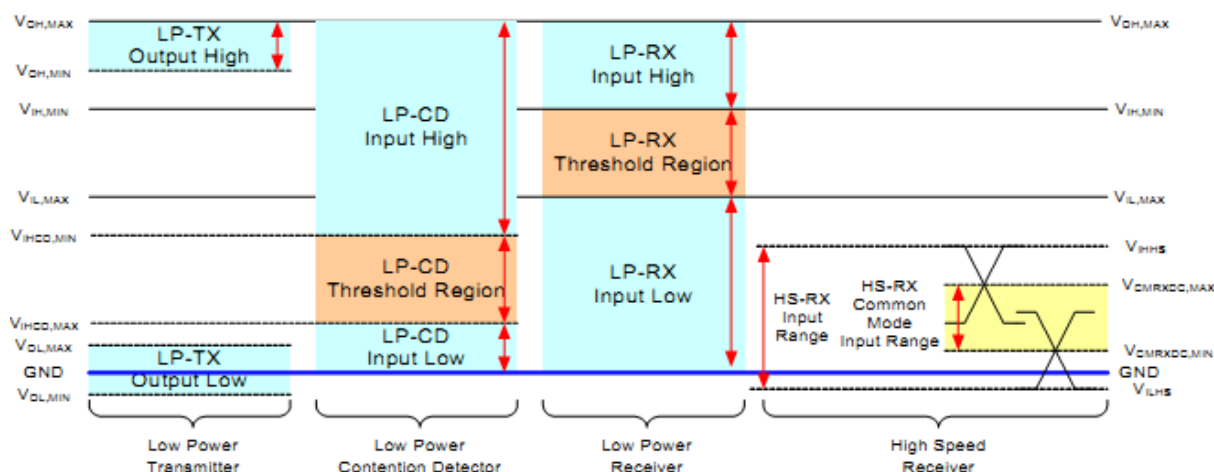
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6. Reliability Test Conditions And Methods

NO	Item	Condition	Method
1	High / Low Temperature Storage	80℃/-30℃ 120hrs	Check and record every 96Hrs
2	High / Low Temperature Life	70℃/-20℃ 120hrs (operating mode)	Check and record every 96Hrs
3	High Temperature、High Humidity Operating	40℃ 90% RH, 120Hrs	Check and record every 48hrs
4	Thermal Shock	-30℃(30Min) → 25℃(5Min) → 80℃(30Min) (conversion time, : 5 sec) 20 cycles	Each 10 cycles end , check
5	Vibration	10Hz~55Hz~10Hz Amplitude: 1.5mm 2hrs for each direction(X,Y,Z)	Each direction end, Check the Appearance and Electrical Characteristics
6	Static Electricity	Gap mood: ±1KV~±8KV (10 times air discharge with positive/negative voltage voltage gap : 1kv) Touch mood: ±1KV~±2KV	Each discharge end, Check the Electrical Characteristics
7	Slump	Free faller movement for each side、cording、angle (75cm High、 6 sides、 2 angle、 2 cording)	End

7. MIPI DC Characteristics

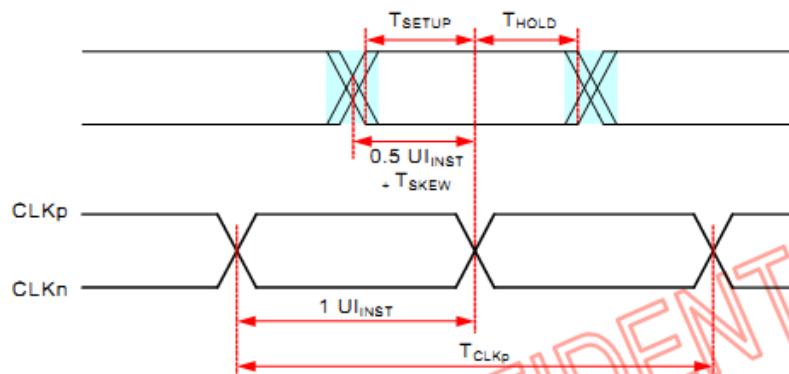
Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.65	1.8	3.6	V
VP_HSSI	High speed / Low power mode operating voltage		1.62		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
VOD	HS transmit differential voltage ($VOD = VDP - VDN$)	140	200	250	mV
V _{OTH}	Different input high threshold			70	mV
V _{OTL}	Different input low threshold	-70			mV
V _{TERM-EN}	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0.0		550	mV
VIH	Logic 1 input threshold	680		VDDAM	mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD,MAX	Logic 0 contention threshold	0.0		200	mV
VILCD,MIN	Logic 1 contention threshold	450		VDDAM	mV



8. Timing Characteristics

7.3.1 MIPI Interface Characteristics

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2,10
Data to Clock Skew [measured at transmitter]	$T_{SKEW}[TX]$	-0.15		0.15	UI_{INST}	3
		-0.2		0.2	UI_{INST}	4
Data to Clock Setup Time [measured at receiver]	$T_{SETUP}[RX]$	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
Data to Clock Hold Time [measured at receiver]	$T_{HOLD}[RX]$	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
20% - 80% rise time and fall time	t_r / t_f	100			ps	9
				0.3	UI_{INST}	7
				0.35	UI_{INST}	8

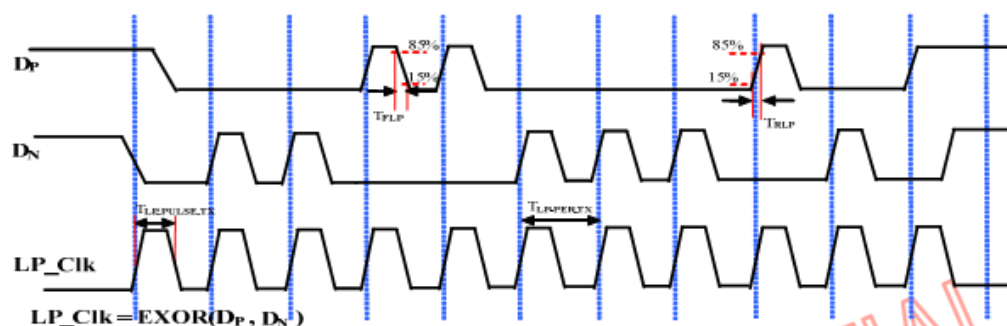
Note:

- This value corresponds to a minimum 80 MHz data rate.
- The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
- Total silicon and package delay budget of $0.3 \cdot UI_{INST}$ when D-PHY is supporting maximum data rate = 1Gbps.
- Total silicon and package delay budget of $0.4 \cdot UI_{INST}$ when D-PHY is supporting maximum data rate > 1Gbps.
- Total setup and hold window for receiver of $0.3 \cdot UI_{INST}$ when D-PHY is supporting maximum data rate = 1Gbps.
- Total setup and hold window for receiver of $0.4 \cdot UI_{INST}$ when D-PHY is supporting maximum data rate > 1Gbps.
- Applicable when operating at HS bit rates ≤ 1 Gbps ($UI \geq 1$ ns).
- Applicable when operating at HS bit rates > 1 Gbps ($UI < 1$ ns).
- Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps ($UI \geq 1$ ns), should not use values below 150 ps.
- For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for 5-5-5.

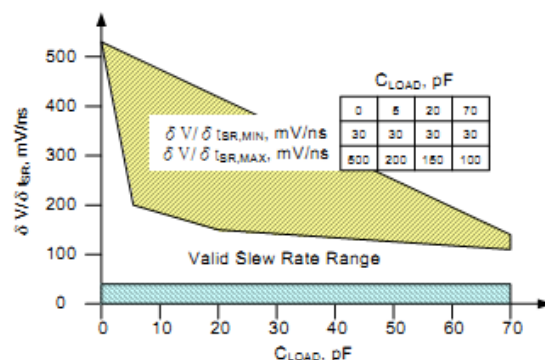
LP Transmission AC Specification



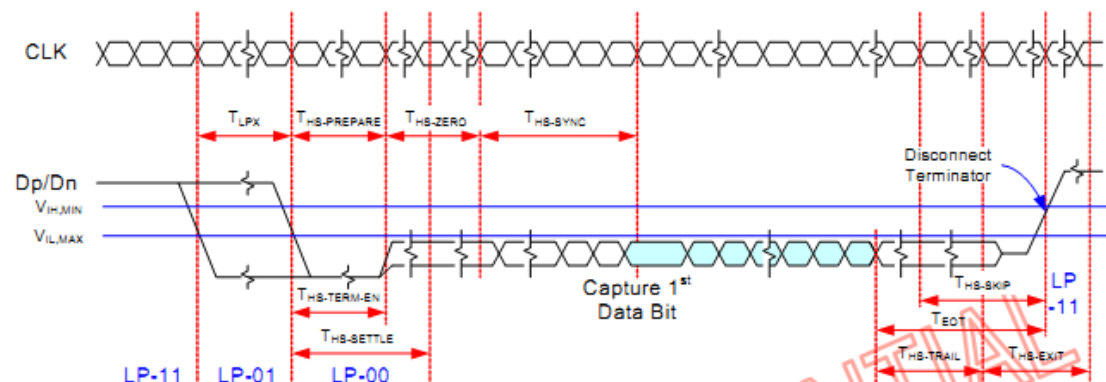
Parameter	Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time	T_{RLP} / T_{FLP}			25	ns	1
30%-85% rise time and fall time	T_{REOT}			35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	40			ns	4
	All other pulses	20			ns	4
Period of the LP exclusive-OR clock	$T_{LP_PER_TX}$	90			ns	
Slew Rate@ $C_{LOAD} = 0pF$	$\delta V / \delta t_{tr}$	30		500	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 5pF$		30		200	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 20pF$		30		150	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 70pF$		30		100	mV/ns	1,2,3,7
Load Capacitance	C_{LOAD}			70	pF	1

Note:

- C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be $<10pF$. The distributed line capacitance can be up to $50pF$ for a transmission line with $2ns$ delay.
- When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
- Measured as average across any 50 mV segment of the output signal transition.
- This parameter value can be lower than $TLPX$ due to differences in rise vs. fall signal slopes and trip levels and mismatches between D_p and D_n LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.
- The rise-time of $TREOT$ starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
- With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.
- This value represents a corner point in a piecewise linear curve as bellowed.



High-Speed Data Transmission in Bursts

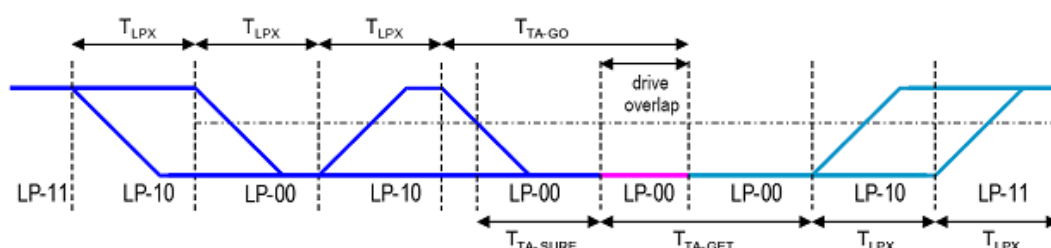


Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of $T_{HS-TRAIL}$ or $tCLK-TRAIL$ period to start of LP-11 state	T_{EoT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Note:

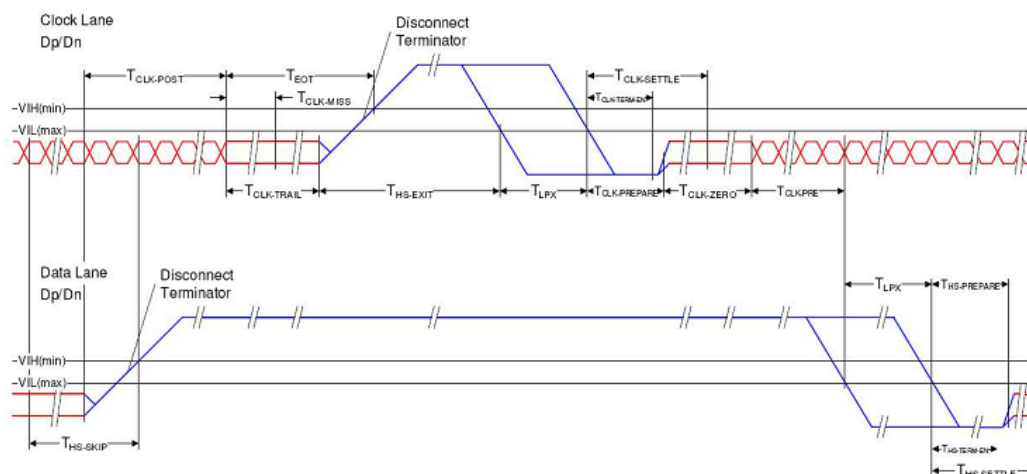
- 1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
- 2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
- 3: T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of $T_{LPX}(MASTER)/T_{LPX}(SLAVE)$ between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+128UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERMIN}$			38	ns
Minimum time that the HS clock must be set prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

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9. Power Supply Configuration

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	4.8	V	Note 1
I/O operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.6	V	Note 1
Analog Operating voltage	AVDD	Operating Voltage	GVDDP+0.5		6	V	Note 5
Analog Operating voltage	AVEE	Operating Voltage	-6		GVDDN-0.5	V	Note 6
MIPI Operating voltage	VDDAM	MIPI Supply voltage	1.65	1.8	3.6	V	Note1
Input / Output							
Logic High level input voltage	VIH		0.7VDDI	-	VDDI	V	Note 1, 2
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2
Logic High level output voltage	VOH	IOH ▯ -0.1mA	0.8VDDI	-	VDDI	V	Note 1, 2
Logic Low level output voltage	VOL	IOL ▯ +0.1mA	VSS	-	0.2VDDI	V	Note 1, 2
Logic High level leakage (Except MIPI)	ILIH1	Vin ▯ 0 to VDDI			1	uA	Note 1, 2
Logic Low level leakage (Except MIPI)	ILIL1	Vin ▯ 0 to VDDI	-1			uA	Note 1, 2
Logic High level leakage MIPI	ILIH2	Vin ▯ 0 to 1.3 V			10	uA	
Logic Low level leakage MIPI	ILIL2	Vin ▯ 0 to 1.3 V	-10			uA	
VCOM Operation							
VCOMDC voltage	VCOMDC3	Operating Voltage	-4		+1	V	
Source Driver							
Gamma reference voltage	GVDDP	GVDDP>AVDD-0.3	3.5	-	5.5	V	Note3
	GVDDN	GVDDN>AVEE+0.3	-5.5		3.5	V	
Output deviation voltage	V.dev1	Sout>=+4.2V, Sout<=+0.8V	-	20	30	mV	
	V.dev2	+0.8V<Sout<+4.2V	-	10	15	mV	
	V.dev3	Sout>=0.8V, Sout<=-4.2V		20	30	mV	
	V.dev4	-0.8V<Sout<-4.2V		10	15	mV	
Output offset voltage	VDFSET				35	mv	
Power generation							
Internal reference voltage	VREF	Operating Voltage		1.2		V	
Power supply for Digital circuit	VDD			1.62		V	
Power supply for MIPI I/F	VP_HSSI			1.62		V	
Analog power	AVDD		4.5		6	V	
Analog power	AVEE		-6		-4.5	V	
LDO output for GVDDP	AVDDR		3		5.5	V	
LDO output for GVDDN	AVEER		-5.5		-3	V	
LDO output for VGH	VGHO	VGH > VGHO + 0.3V	7		20	V	Note 4
LDO output for VGL	VGLO	VGL < VGLO-0.3V	-4		-18	V	Note 4
1st Booster voltage	VGH	Operating Voltage	2xAVDD		3xAVDD-AVEE	V	
2nd Booster voltage	VGL	Operating Voltage	2*AVEE -AV DD		AVEE - VCI1	V	
3rd Booster voltage or LDO output	VCL	Operating Voltage from pump Circuit or LDO	-3.3		-2.5	V	
Oscillator tolerance	OSC	25℃	-3	-	3	%	
Oscillator tolerance	OSC	75℃~30℃	-5	-	5	%	

Note 1: VDDI=1.65 to 3.6V, VCI= 2.5 to 4.8V, VDDAM=1.65 to 3.6 V, AVSS=VSS=0V, Ta=-30 to 75 ℃ (to +85 ℃ no damage)

Note 2: When the measurements are performed with LCD module, Measurement Points are like below.

CSX, RDY, WRX, D[23:0], DCX, RESX, SCL, IM[2 : 0] and Test pins

Note 3: Source channel loading= 40pF/channel

Note 4: VCI=3.3V, Ta=25 ℃, No load;

Note 5: for 2-2 power mode, 3-power mode and 4-power mode usage only

Note 6: for 3-power mode and 4-power mode usage only

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10.Optical Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ_{21} θ_{22}	-	80	-	Deg.	[Note1,5]
	Vertical	θ_{11} θ_{12}		80	-	Deg.	
Brightness	Br	$\theta=0$ deg.	-	-	-	nits	[Note 2]
Contrast ratio	CR		700	1000	-	-	[Note3,5]
Response time	τ_{DRV}		-	-	35	ms	[Note4,5,6]
Cell Transparency	Tr		-	-	-	%	[Note 5]
Chromaticity of white	x		Typ.-0.03	TBD	Typ.+0.03	-	[Note 5]
	y		Typ.-0.03	TBD	Typ.+0.03	-	
Chromaticity of red	x		Typ.-0.03	TBD	Typ.+0.03	-	
	y		Typ.-0.03	TBD	Typ.+0.03	-	
Chromaticity of green	x		Typ.-0.03	TBD	Typ.+0.03	-	
	y		Typ.-0.03	TBD	Typ.+0.03	-	
Chromaticity of blue	x		Typ.-0.03	TBD	Typ.+0.03	-	
	y		Typ.-0.03	TBD	Typ.+0.03	-	
Transmittance	Tr%	-	-	(4.24)	-	-	With APCF
Uniformity	%	-	-	80	-	-	[Note 7]
Crosstalk	CT	-	-	-	4	%	[Note 8]
Color temperature variation	δT_c	-	-	-	1.1	-	[Note 5,9]

[Note 1] Definitions of viewing angle range:

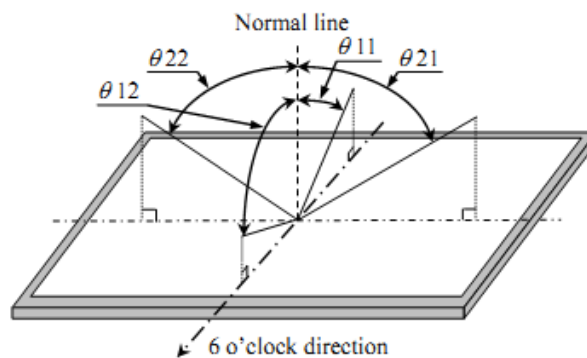
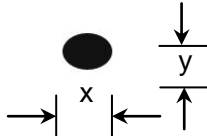
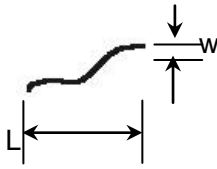


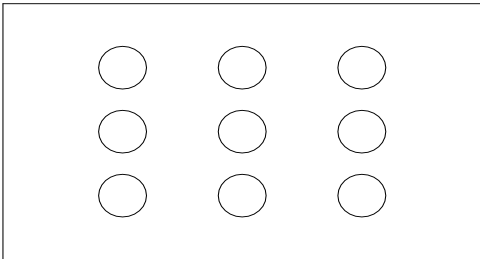
Fig.8-1 Viewing angle

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11.Inspection Standard

No	Item	Criterion																		
01	Outline Dimension	In accord with drawing																		
02	Position-finding Dimension Assemble Dimension	In accord with drawing																		
03	LCD black spots, white spots (Round type)	Round type: non display Unit : mm  <table><tr><th>Dimension</th><th>Qualified Quantity</th></tr><tr><td>$D \leq 0.1$</td><td>Ignore</td></tr><tr><td>$0.1 < D \leq 0.15$</td><td>3</td></tr><tr><td>$0.15 < D \leq 0.25$</td><td>2</td></tr><tr><td>$D > 0.25$</td><td>0</td></tr></table>	Dimension	Qualified Quantity	$D \leq 0.1$	Ignore	$0.1 < D \leq 0.15$	3	$0.15 < D \leq 0.25$	2	$D > 0.25$	0								
		Dimension	Qualified Quantity																	
$D \leq 0.1$	Ignore																			
$0.1 < D \leq 0.15$	3																			
$0.15 < D \leq 0.25$	2																			
$D > 0.25$	0																			
04	LCD black spots, white spots (Line Style)	Unit : mm  <table><tr><th>Length</th><th>Width</th><th>Qualified Quantity</th></tr><tr><td>-</td><td>≤ 0.02</td><td>Ignore</td></tr><tr><td>≤ 3</td><td rowspan="2">$0.02 < W \leq 0.03$</td><td>2</td></tr><tr><td></td><td></td></tr><tr><td>≤ 2</td><td>$0.03 < W \leq 0.05$</td><td>1</td></tr><tr><td>-</td><td>$D > 0.05$</td><td>According to circle</td></tr></table>	Length	Width	Qualified Quantity	-	≤ 0.02	Ignore	≤ 3	$0.02 < W \leq 0.03$	2			≤ 2	$0.03 < W \leq 0.05$	1	-	$D > 0.05$	According to circle	
		Length	Width	Qualified Quantity																
		-	≤ 0.02	Ignore																
		≤ 3	$0.02 < W \leq 0.03$	2																
		≤ 2	$0.03 < W \leq 0.05$	1																
-	$D > 0.05$	According to circle																		

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05	LCD Scratch 、 Threadlike Fiber	Same to NO.3 circle sightline and surface of LCD is vertical (2)Same to NO.3 line style		
06	POL	It is not admissible that POL is beyond the edge of glass, else, unqualified. It is essential that POL is over the 50 percent of width of frame , else ,unqualified. According to the drawing in case of special definition.		
07	Brightness	In accord with product specification	Drive condition is according to specification Measure location is in Follow Picture 3 、 Adjust brightness instrument to zero , burrow against the surface of LCD , press “measure” , record when the display is steady. (YOKOGAWA-3298)	
			 <p>Measure location</p>	
08	CR (Max)	According to specification	According to product specification Measure instrument (DMS-501)	
09	Response time	According to specification	According to product specification Measure instrument (DMS-501)	
10	Viewing angle	According to specification	According to product specification Measure instrument (DMS-501)	
11	Vibration、 Ring	Compare with the sample customer supply	Compare with the sample customer supply when assemble	

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12 . Handling Precautions

12.1 Mounting method

The LCD panel of SC LCD LCD module consists of two thin glass plates with polarizes which easily be damaged. And since the module is so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent [recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being sili8con coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 packing

- Module employ LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.

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- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
[It is recommended to store them as they have been contained in the inner container at the time of delivery from us

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

13. Precaution For Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to SC LCD , and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14 Packing Method

To Be Determined